

What is claimed is:

1. A method of forming a gate dielectric on a transistor body region, comprising:  
 evaporating  $\text{Al}_2\text{O}_3$  at a first rate;  
 evaporating  $\text{La}_2\text{O}_3$  at a second rate; and  
 controlling the first rate and the second rate to provide a film containing  $\text{LaAlO}_3$   
 on the transistor body region.
2. The method of claim 1, wherein evaporating  $\text{Al}_2\text{O}_3$  and evaporating  $\text{La}_2\text{O}_3$   
 includes evaporating dry pellets of  $\text{Al}_2\text{O}_3$  and  $\text{La}_2\text{O}_3$ .
3. The method of claim 1, wherein evaporating  $\text{La}_2\text{O}_3$  includes evaporating  $\text{La}_2\text{O}_3$  by  
 electron beam evaporation.
4. The method of claim 1, wherein controlling the first rate and the second rate  
 includes controlling the first rate and the second rate to selectively provide a film  
 composition having a predetermined dielectric constant.
5. The method of claim 4, wherein selectively providing a film composition having a  
 predetermined dielectric constant includes providing a film composition with a dielectric  
 constant ranging from the dielectric constant of an  $\text{Al}_2\text{O}_3$  film to the dielectric constant of  
 a  $\text{La}_2\text{O}_3$  film.
6. The method of claim 1, wherein controlling the first rate and the second rate to  
 provide a film containing  $\text{LaAlO}_3$  includes providing an amorphous  $\text{LaAlO}_3$  film.
7. The method of claim 1, wherein evaporating  $\text{La}_2\text{O}_3$  begins substantially  
 concurrent with beginning evaporating  $\text{Al}_2\text{O}_3$ .

8. The method of claim 1, wherein evaporating  $\text{Al}_2\text{O}_3$  and evaporating  $\text{La}_2\text{O}_3$  includes depositing  $\text{LaAlO}_3$  on the transistor body region in a base pressure lower than about  $5 \times 10^{-7}$  Torr and in a deposition pressure lower than about  $2 \times 10^{-6}$  Torr.
9. The method of claim 1, further including annealing the transistor body region after providing the film containing  $\text{LaAlO}_3$ .
10. The method of claim 9, wherein annealing the transistor body region after providing the film containing  $\text{LaAlO}_3$  includes annealing in  $\text{N}_2$ .
11. The method of claim 10, wherein annealing in  $\text{N}_2$  includes annealing in an electric furnace at about  $700^\circ\text{C}$ .
12. The method of claim 10, wherein annealing in  $\text{N}_2$  includes annealing in RTA in the range from about  $800^\circ\text{C}$  to about  $900^\circ\text{C}$ .
13. A method of forming a gate dielectric on a transistor body region, comprising:  
evaporating  $\text{Al}_2\text{O}_3$  at a first rate using a first electron gun;  
evaporating  $\text{La}_2\text{O}_3$  at a second rate using a second electron gun; and  
controlling the first rate and the second rate to provide a film containing  $\text{LaAlO}_3$  on the transistor body region.
14. The method of claim 13, wherein evaporating  $\text{Al}_2\text{O}_3$  and evaporating  $\text{La}_2\text{O}_3$  includes evaporating dry pellets of  $\text{Al}_2\text{O}_3$  and  $\text{La}_2\text{O}_3$ .
15. The method of claim 13, wherein controlling the first rate and the second rate includes controlling the first rate and the second rate to selectively provide a film composition having a predetermined dielectric constant.

16. The method of claim 15, wherein selectively providing a film composition having a predetermined dielectric constant includes providing a film composition with a dielectric constant ranging from the dielectric constant of an  $\text{Al}_2\text{O}_3$  film to the dielectric constant of a  $\text{La}_2\text{O}_3$  film.
17. The method of claim 13, wherein controlling the first rate and the second rate to provide a film containing  $\text{LaAlO}_3$  includes providing an amorphous  $\text{LaAlO}_3$  film.
18. The method of claim 13, wherein evaporating  $\text{La}_2\text{O}_3$  begins substantially concurrent with beginning evaporating  $\text{Al}_2\text{O}_3$ .
19. The method of claim 13, wherein forming the gate dielectric includes growing the film containing  $\text{LaAlO}_3$  at a growth rate in the range from about 0.5 nm/min to about 50 nm/min.
20. The method of claim 13, further including annealing the transistor body region after providing the film containing  $\text{LaAlO}_3$ .
21. A method of forming a gate dielectric on a transistor body region, comprising:
  - evaporating  $\text{Al}_2\text{O}_3$  at a first rate using a first electron gun;
  - evaporating  $\text{La}_2\text{O}_3$  at a second rate using a second electron gun;
  - controlling the first rate and the second rate to provide a film containing  $\text{LaAlO}_3$  on the transistor body region; and
  - annealing in  $\text{N}_2$  after providing the film containing  $\text{LaAlO}_3$  on the transistor body region.
22. The method of claim 21, wherein evaporating  $\text{Al}_2\text{O}_3$  and evaporating  $\text{La}_2\text{O}_3$  includes evaporating dry pellets of  $\text{Al}_2\text{O}_3$  and  $\text{La}_2\text{O}_3$ .

23. The method of claim 21, wherein controlling the first rate and the second rate includes controlling the first rate and the second rate to selectively provide a film composition having a predetermined dielectric constant.
24. The method of claim 21, wherein controlling the first rate and the second rate to provide a film containing  $\text{LaAlO}_3$  includes providing an amorphous  $\text{LaAlO}_3$  film.
25. The method of claim 21, wherein evaporating  $\text{La}_2\text{O}_3$  begins substantially concurrent with beginning evaporating  $\text{Al}_2\text{O}_3$ .
26. The method of claim 21, wherein evaporating  $\text{Al}_2\text{O}_3$  and evaporating  $\text{La}_2\text{O}_3$  includes depositing  $\text{LaAlO}_3$  on the transistor body region in a base pressure lower than about  $5 \times 10^{-7}$  Torr and in a deposition pressure lower than about  $2 \times 10^{-6}$  Torr.
27. The method of claim 21, wherein annealing in  $\text{N}_2$  includes annealing in an electric furnace at about  $700^\circ\text{C}$ .
28. The method of claim 21, wherein forming the gate dielectric includes growing the film containing  $\text{LaAlO}_3$  at a growth rate in the range from about 0.5 nm/min to about 50 nm/min.
29. A method of forming a transistor, comprising:
  - forming first and second source/drain regions;
  - forming a body region between the first and second source/drain regions;
  - evaporating  $\text{Al}_2\text{O}_3$  at a first rate;
  - evaporating  $\text{La}_2\text{O}_3$  at a second rate;
  - controlling the first rate and the second rate to provide a film containing  $\text{LaAlO}_3$  on the body region; and
  - coupling a gate to the film containing  $\text{LaAlO}_3$ .

30. The method of claim 29, wherein evaporating  $\text{Al}_2\text{O}_3$  and evaporating  $\text{La}_2\text{O}_3$  includes evaporating dry pellets of  $\text{Al}_2\text{O}_3$  and  $\text{La}_2\text{O}_3$ .
31. The method of claim 29, wherein controlling the first rate and the second rate includes controlling the first rate and the second rate to selectively provide a film composition having a predetermined dielectric constant.
32. The method of claim 29, wherein selectively providing a film composition having a predetermined dielectric constant includes providing a film composition with a dielectric constant ranging from the dielectric constant of an  $\text{Al}_2\text{O}_3$  film to the dielectric constant of a  $\text{La}_2\text{O}_3$  film.
33. The method of claim 29, wherein controlling the first rate and the second rate to provide a film containing  $\text{LaAlO}_3$  includes providing an amorphous  $\text{LaAlO}_3$  film.
34. The method of claim 29, wherein evaporating  $\text{La}_2\text{O}_3$  begins substantially concurrent with beginning evaporating  $\text{Al}_2\text{O}_3$ .
35. A method of forming a memory array, comprising:
  - forming a number of access transistors, comprising:
    - forming first and second source/drain regions;
    - forming a body region between the first and second source/drain regions;
    - evaporating  $\text{Al}_2\text{O}_3$  at a first rate;
    - evaporating  $\text{La}_2\text{O}_3$  at a second rate;
    - controlling the first rate and the second rate to provide a film containing  $\text{LaAlO}_3$  on the body region. ; and
    - coupling a gate to the film containing  $\text{LaAlO}_3$ ;

forming a number of wordlines coupled to a number of the gates of the number of access transistors;

forming a number of sourcelines coupled to a number of the first source/drain regions of the number of access transistors; and

forming a number of bitlines coupled to a number of the second source/drain regions of the number of access transistors.

36. The method of claim 35, wherein evaporating  $\text{Al}_2\text{O}_3$  and evaporating  $\text{La}_2\text{O}_3$  includes evaporating dry pellets of  $\text{Al}_2\text{O}_3$  and  $\text{La}_2\text{O}_3$ .

37. The method of claim 35, wherein controlling the first rate and the second rate includes controlling the first rate and the second rate to selectively provide a film composition having a predetermined dielectric constant.

38. The method of claim 37, wherein selectively providing a film composition having a predetermined dielectric constant includes providing a film composition with a dielectric constant ranging from the dielectric constant of an  $\text{Al}_2\text{O}_3$  film to the dielectric constant of a  $\text{La}_2\text{O}_3$  film.

39. The method of claim 35, wherein forming the gate dielectric includes growing the film containing  $\text{LaAlO}_3$  at a growth rate in the range from about 0.5 nm/min to about 50 nm/min.

40. A method of forming an information handling system, comprising:  
forming a processor;  
forming a memory array, comprising:  
forming a number of access transistors, comprising:  
forming first and second source/drain regions;

forming a body region between the first and second source/drain regions;

evaporating  $\text{Al}_2\text{O}_3$  at a first rate;

evaporating  $\text{La}_2\text{O}_3$  at a second rate;

controlling the first rate and the second rate to provide a film containing  $\text{LaAlO}_3$  on the body region. ; and

coupling a gate to the film containing  $\text{LaAlO}_3$ ;

forming a number of wordlines coupled to a number of the gates of the number of access transistors;

forming a number of sourcelines coupled to a number of the first source/drain regions of the number of access transistors;

forming a number of bitlines coupled to a number of the second source/drain regions of the number of access transistors; and

forming a system bus that couples the processor to the memory array.

41. The method of claim 40, wherein evaporating  $\text{Al}_2\text{O}_3$  and evaporating  $\text{La}_2\text{O}_3$  includes evaporating dry pellets of  $\text{Al}_2\text{O}_3$  and  $\text{La}_2\text{O}_3$ .

42. The method of claim 40, wherein evaporating  $\text{La}_2\text{O}_3$  and evaporating  $\text{Al}_2\text{O}_3$  includes evaporating  $\text{La}_2\text{O}_3$  and evaporating  $\text{Al}_2\text{O}_3$  by electron beam evaporation.

43. The method of claim 40, wherein controlling the first rate and the second rate includes controlling the first rate and the second rate to selectively provide a film composition having a predetermined dielectric constant.

44. A transistor, comprising:

a first and second source/drain region;

a body region located between the first and second source/drain regions;

a dielectric layer containing  $\text{LaAlO}_3$  coupled to a surface portion of the body region between the first and second source/drain regions, the dielectric layer including  $\text{Al}_2\text{O}_3$ , or  $\text{La}_2\text{O}_3$ ; and

a gate coupled to the dielectric layer.

45. The transistor of claim 44, wherein the dielectric layer includes  $\text{Al}_2\text{O}_3$ , and  $\text{La}_2\text{O}_3$ .

46. The transistor of claim 44, wherein the dielectric layer is substantially amorphous.

47. The transistor of claim 44, wherein the dielectric layer exhibits a dielectric constant in the range from about 21 to about 25.

48. The transistor of claim 44, wherein the dielectric layer exhibits an equivalent oxide thickness ( $t_{\text{eq}}$ ) in the range from about 1.5 Angstroms to about 5 Angstroms.

49. The transistor of claim 44, wherein the dielectric layer exhibits an equivalent oxide thickness ( $t_{\text{eq}}$ ) of less than 3 Angstroms.

50. A memory array, comprising:

a number of access transistors, comprising:

a first and second source/drain region;

a body region located between the first and second source/drain regions;

a dielectric layer containing  $\text{LaAlO}_3$  coupled to a surface portion of the body region between the first and second source/drain regions, the dielectric layer including  $\text{Al}_2\text{O}_3$ , or  $\text{La}_2\text{O}_3$ ; and

a gate coupled to the dielectric layer;

a number of wordlines coupled to a number of the gates of the number of access transistors;



a number of sourcelines coupled to a number of the first source/drain regions of the number of access transistors; and

a number of bitlines coupled to a number of the second source/drain regions of the number of access transistors.

51. The memory array of claim 50, wherein the dielectric layer includes  $\text{Al}_2\text{O}_3$ , and  $\text{La}_2\text{O}_3$ .

52. The memory array of claim 50, wherein the dielectric layer is substantially amorphous.

53. The memory array of claim 50, wherein the dielectric layer exhibits a dielectric constant in the range from about 21 to about 25.

54. The memory array of claim 50, wherein the dielectric layer exhibits an equivalent oxide thickness ( $t_{\text{eq}}$ ) in the range from about 1.5 Angstroms to about 5 Angstroms.

55. The memory array of claim 50, wherein the dielectric layer exhibits an equivalent oxide thickness ( $t_{\text{eq}}$ ) of less than 3 Angstroms.

56. An information handling device, comprising:

a processor;

a memory array, comprising:

a number of access transistors, comprising:

a first and second source/drain region;

a body region located between the first and second source/drain

regions;

a dielectric layer containing  $\text{LaAlO}_3$  coupled to a surface portion of the body region between the first and second source/drain regions, the dielectric layer including  $\text{Al}_2\text{O}_3$ , or  $\text{La}_2\text{O}_3$ ; and

a gate coupled to the dielectric layer;

a number of wordlines coupled to a number of the gates of the number of access transistors;

a number of sourcelines coupled to a number of the first source/drain regions of the number of access transistors;

a number of bitlines coupled to a number of the second source/drain regions of the number of access transistors; and

a system bus coupling the processor to the memory device.

57. The information handling device of claim 56, wherein the dielectric layer includes  $\text{Al}_2\text{O}_3$ , and  $\text{La}_2\text{O}_3$ .

58. The information handling device of claim 56, wherein the dielectric layer is substantially amorphous.

59. The information handling device of claim 56, wherein the dielectric layer exhibits a dielectric constant in the range from about 21 to about 25.

60. The information handling device of claim 56, wherein the dielectric layer exhibits an equivalent oxide thickness ( $t_{\text{eq}}$ ) in the range from about 1.5 Angstroms to about 5 Angstroms.

61. The information handling device of claim 56, wherein the dielectric layer exhibits an equivalent oxide thickness ( $t_{\text{eq}}$ ) of less than 3 Angstroms.

62. A transistor formed by the process, comprising:  
forming a body region coupled between a first source/drain region and a second source/drain region;  
evaporating  $\text{Al}_2\text{O}_3$  at a first rate;  
evaporating  $\text{La}_2\text{O}_3$  at a second rate;  
controlling the first rate and the second rate to provide a film containing  $\text{LaAlO}_3$  on the body region; and  
coupling a gate to the film containing  $\text{LaAlO}_3$ .
63. The transistor of claim 62, wherein evaporating  $\text{Al}_2\text{O}_3$  and evaporating  $\text{La}_2\text{O}_3$  includes evaporating dry pellets of  $\text{Al}_2\text{O}_3$  and  $\text{La}_2\text{O}_3$ .
64. The transistor of claim 62, wherein evaporating  $\text{Al}_2\text{O}_3$  and evaporating  $\text{La}_2\text{O}_3$  includes evaporating  $\text{Al}_2\text{O}_3$  using a first electron gun and evaporating  $\text{La}_2\text{O}_3$  using a second electron gun.
65. The transistor of claim 62, wherein controlling the first rate and the second rate includes controlling the first rate and the second rate to selectively provide a film composition having a predetermined dielectric constant.
66. The transistor of claim 62, wherein the dielectric layer exhibits a dielectric constant in the range from about 21 to about 25.
67. The transistor of claim 62, wherein the dielectric layer exhibits an equivalent oxide thickness ( $t_{\text{eq}}$ ) in the range from about 1.5 Angstroms to about 5 Angstroms.